74LVC1G74

Single D-type flip-flop with set and reset; positive edge trigger

Rev. 06 — 19 February 2008 Product data sheet

1. General description

The 74LVC1G74 is a single positive edge triggered D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set ($\overline{SD}$) and reset ($\overline{RD}$) inputs, and complementary Q and $\overline{Q}$ outputs.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing damaging backflow current through the device when it is powered down.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

2. Features

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant inputs for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ±24 mA output drive (V_{CC} = 3.0 V)
- ESD protection:
  - HBM EIA/JESD22-A114E exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G74DP	–40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC1G74DC	–40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC1G74GT	–40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74LVC1G74GM	–40 °C to +125 °C	XQFN8U	plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 × 1.6 × 0.5 mm	SOT902-1

4. Marking

Table 2. Marking codes

Type number	Marking code
74LVC1G74DP	V74
74LVC1G74DC	V74
74LVC1G74GT	V74
74LVC1G74GM	V74

5. Functional diagram

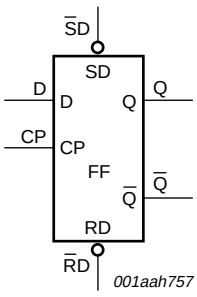


Fig 1. Logic symbol

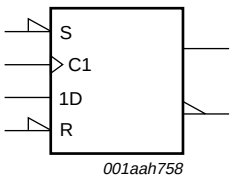


Fig 2. IEC logic symbol

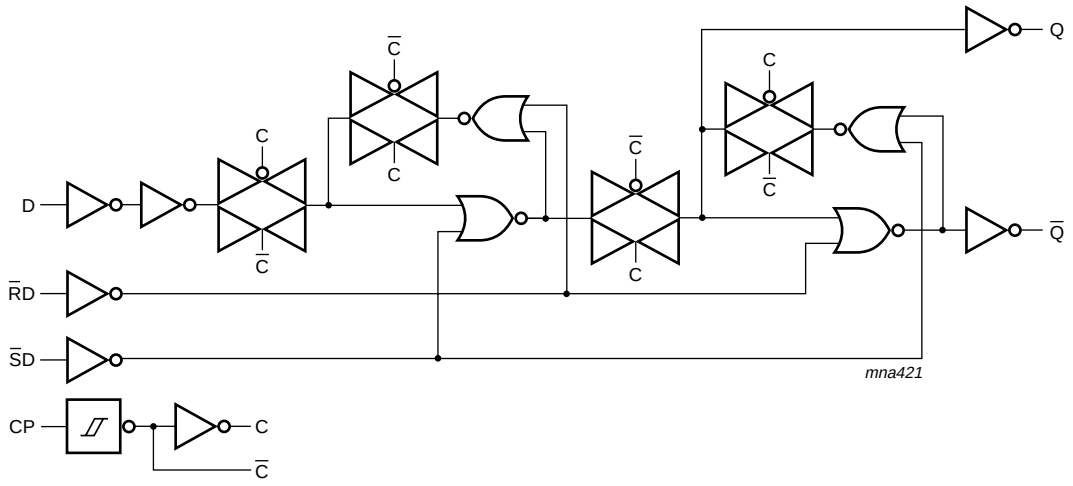


Fig 3. Logic diagram

6. Pinning information

6.1 Pinning

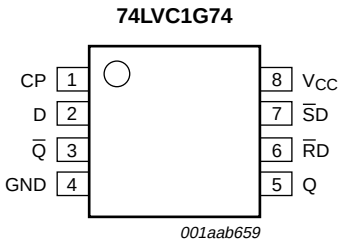
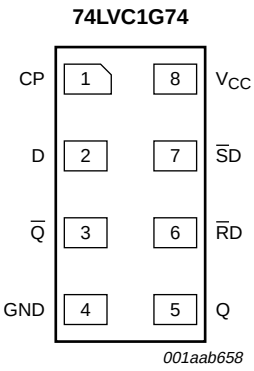
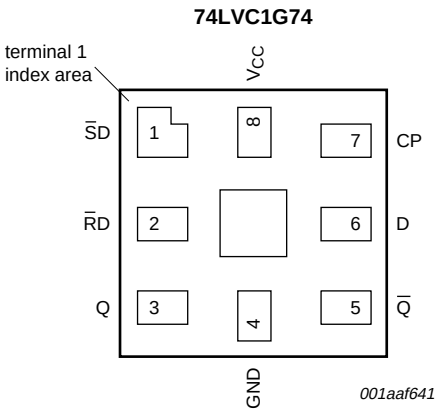


Fig 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)



Transparent top view

Fig 5. Pin configuration SOT833-1 (XSON8)



Transparent top view

Fig 6. Pin configuration SOT902-1 (XQFN8U)

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT505-2, SOT765-1, SOT833-1	SOT902-1	
CP	1	7	clock input (LOW-to-HIGH, edge-triggered)
D	2	6	data input
$\overline{Q}$	3	5	complement output
GND	4	4	ground (0 V)
Q	5	3	true output
$\overline{RD}$	6	2	asynchronous reset-direct input (active LOW)
$\overline{SD}$	7	1	asynchronous set-direct input (active LOW)
V_{CC}	8	8	supply voltage

7. Functional description

Table 4. Function table for asynchronous operation[1]

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

Table 5. Function table for synchronous operation[1]

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH CP transition;
Q_{n+1} = state after the next LOW-to-HIGH CP transition.

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		–50	-	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	Active mode	[1]	–0.5	V_{CC} + 0.5	V
		Power-down mode	[1][2]	–0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			–100	-	mA
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[3]	-	300	mW
T_{stg}	storage temperature			–65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For TSSOP8 packages: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.
For VSSOP8 packages: above 110 °C the value of P_{tot} derates linearly with 8.0 mW/K.
For XSON8 and XQFN8U packages: above 45 °C the value of P_{tot} derates linearly with 2.4 mW/K.

9. Recommended operating conditions

Table 7. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	5.5	V
T_{amb}	ambient temperature		–40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	-	10	ns/V

10. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −100 µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} − 0.1	-	-	V
		I_O = −4 mA; V_{CC} = 1.65 V	1.2	1.54	-	V
		I_O = −8 mA; V_{CC} = 2.3 V	1.9	2.15	-	V
		I_O = −12 mA; V_{CC} = 2.7 V	2.2	2.50	-	V
		I_O = −24 mA; V_{CC} = 3.0 V	2.3	2.62	-	V
		I_O = −32 mA; V_{CC} = 4.5 V	3.8	4.11	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V	-	-	0.10	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	0.07	0.45	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	0.12	0.30	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	0.17	0.40	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	0.33	0.55	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	0.39	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	±0.1	±5	µA
I_{OFF}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	-	±0.1	±10	µA
I_{CC}	supply current	V_I = 5.5 V or GND; V_{CC} = 1.65 V to 5.5 V; I_O = 0 A	-	0.1	10	µA
ΔI_{CC}	additional supply current	per pin; V_I = V_{CC} − 0.6 V; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V	-	5	500	µA
C_I	input capacitance		-	4.0	-	pF

Table 8. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −100 µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} − 0.1	-	-	V
		I_O = −4 mA; V_{CC} = 1.65 V	0.95	-	-	V
		I_O = −8 mA; V_{CC} = 2.3 V	1.7	-	-	V
		I_O = −12 mA; V_{CC} = 2.7 V	1.9	-	-	V
		I_O = −24 mA; V_{CC} = 3.0 V	2.0	-	-	V
		I_O = −32 mA; V_{CC} = 4.5 V	3.4	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V	-	-	0.10	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.70	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.60	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.80	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.80	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	±20	µA
I_{OFF}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	-	-	±20	µA
I_{CC}	supply current	V_I = 5.5 V or GND; V_{CC} = 1.65 V to 5.5 V; I_O = 0 A	-	-	40	µA
ΔI_{CC}	additional supply current	per pin; V_I = V_{CC} − 0.6 V; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V	-	-	5000	µA

[1] All typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 9.

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	CP to Q, $\overline{Q}$; see Figure 7 [2]						
		V_{CC} = 1.65 V to 1.95 V	1.5	6.0	13.4	1.5	13.4	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	3.5	7.1	1.0	7.1	ns
		V_{CC} = 2.7 V	1.0	3.5	7.1	1.0	7.1	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.5	5.9	1.0	5.9	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	2.5	4.1	1.0	4.1	ns
		$\overline{SD}$ to Q, $\overline{Q}$; see Figure 8 [2]						
		V_{CC} = 1.65 V to 1.95 V	1.5	6.0	12.9	1.5	12.9	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	3.5	7.0	1.0	7.0	ns
		V_{CC} = 2.7 V	1.0	3.5	7.0	1.0	7.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.0	5.9	1.0	5.9	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	2.5	4.1	1.0	4.1	ns
		$\overline{RD}$ to Q, $\overline{Q}$; see Figure 8 [2]						
		V_{CC} = 1.65 V to 1.95 V	1.5	5.0	12.9	1.5	12.9	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	3.5	7.0	1.0	7.0	ns
		V_{CC} = 2.7 V	1.0	3.5	7.0	1.0	7.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.0	5.9	1.0	5.9	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	2.5	4.1	1.0	4.1	ns
t_W	pulse width	CP HIGH or LOW; see Figure 7						
		V_{CC} = 1.65 V to 1.95 V	6.2	-	-	6.2	-	ns
		V_{CC} = 2.3 V to 2.7 V	2.7	-	-	2.7	-	ns
		V_{CC} = 2.7 V	2.7	-	-	2.7	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.7	1.3	-	2.7	-	ns
		V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	ns
		$\overline{SD}$ and $\overline{RD}$ LOW; see Figure 8						
		V_{CC} = 1.65 V to 1.95 V	6.2	-	-	6.2	-	ns
		V_{CC} = 2.3 V to 2.7 V	2.7	-	-	2.7	-	ns
		V_{CC} = 2.7 V	2.7	-	-	2.7	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.7	1.6	-	2.7	-	ns
		V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	ns

Table 9. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 9.

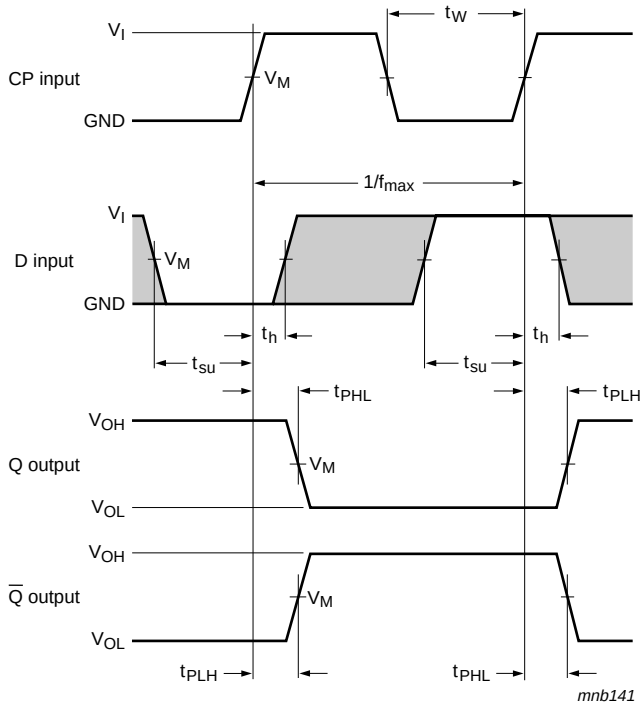
Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{rec}	recovery time	$\overline{SD}$ or $\overline{RD}$; see Figure 8						
		V_{CC} = 1.65 V to 1.95 V	1.9	-	-	1.9	-	ns
		V_{CC} = 2.3 V to 2.7 V	1.4	-	-	1.4	-	ns
		V_{CC} = 2.7 V	1.3	-	-	1.3	-	ns
		V_{CC} = 3.0 V to 3.6 V	+1.2	–3.0	-	+1.2	-	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	-	-	1.0	-	ns
t_{su}	set-up time	D to CP; see Figure 7						
		V_{CC} = 1.65 V to 1.95 V	2.9	-	-	2.9	-	ns
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	ns
		V_{CC} = 2.7 V	1.7	-	-	1.7	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.3	0.5	-	1.3	-	ns
		V_{CC} = 4.5 V to 5.5 V	1.1	-	-	1.1	-	ns
t_h	hold time	D to CP; see Figure 7						
		V_{CC} = 1.65 V to 1.95 V	1.5	-	-	1.5	-	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	-	-	1.0	-	ns
		V_{CC} = 2.7 V	1.0	-	-	1.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	0.6	-	1.0	-	ns
		V_{CC} = 4.5 V to 5.5 V	1.0	-	-	1.0	-	ns
f_{max}	maximum frequency	CP; see Figure 7						
		V_{CC} = 1.65 V to 1.95 V	80	-	-	80	-	MHz
		V_{CC} = 2.3 V to 2.7 V	175	-	-	175	-	MHz
		V_{CC} = 2.7 V	175	-	-	175	-	MHz
		V_{CC} = 3.0 V to 3.6 V	175	280	-	175	-	MHz
		V_{CC} = 4.5 V to 5.5 V	200	-	-	200	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 3.3 V [3]	-	15	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12. Waveforms



Measurement points are given in Table 10.

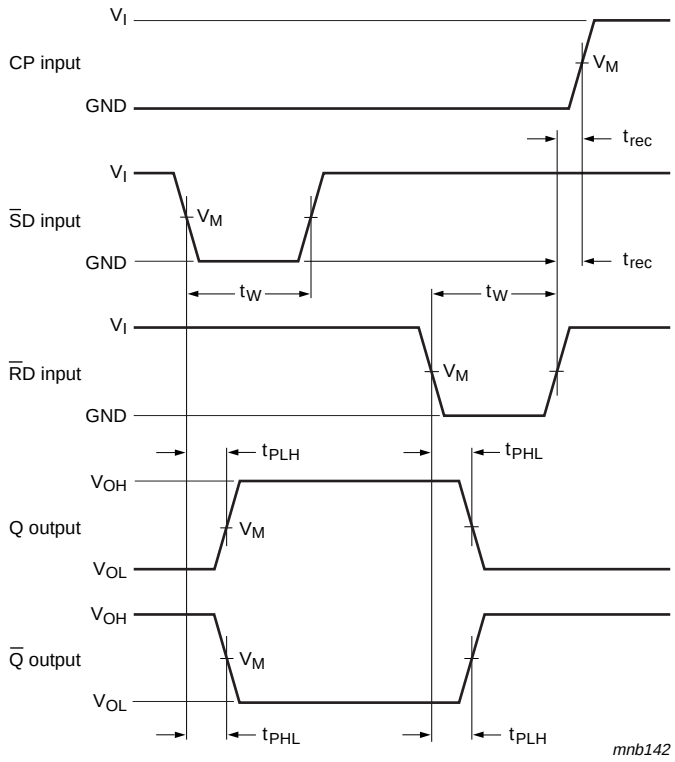
The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. The clock input (CP) to output (Q, $\overline{Q}$) propagation delays, the clock pulse width, the D to CP set-up, the CP to D hold times and the maximum frequency

Table 10. Measurement points

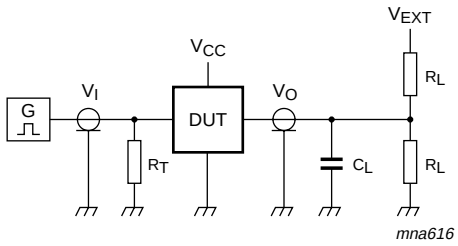
Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. The set ($\overline{SD}$) and reset ($\overline{RD}$) input to output (Q, $\overline{Q}$) propagation delays, the set and reset pulse widths and the $\overline{RD}$ to CP recovery time



Test data is given in Table 11.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

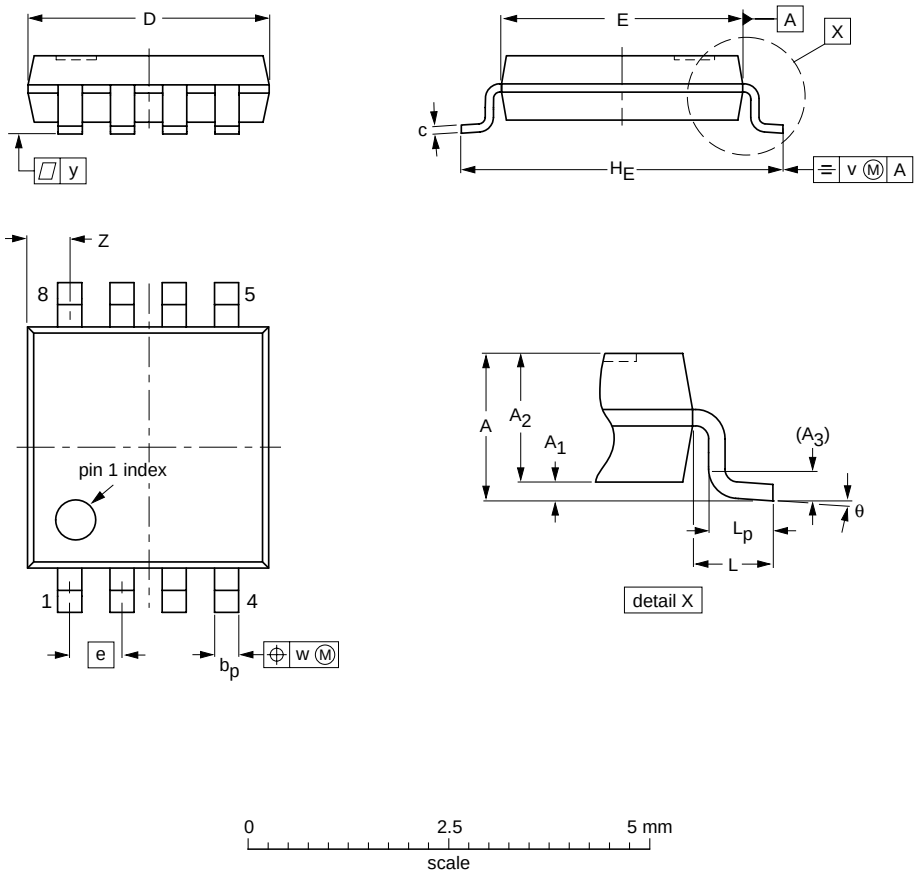
Fig 9. Load circuitry for switching times

Table 11. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open	GND	$2V_{CC}$
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	$2V_{CC}$
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2V_{CC}$

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

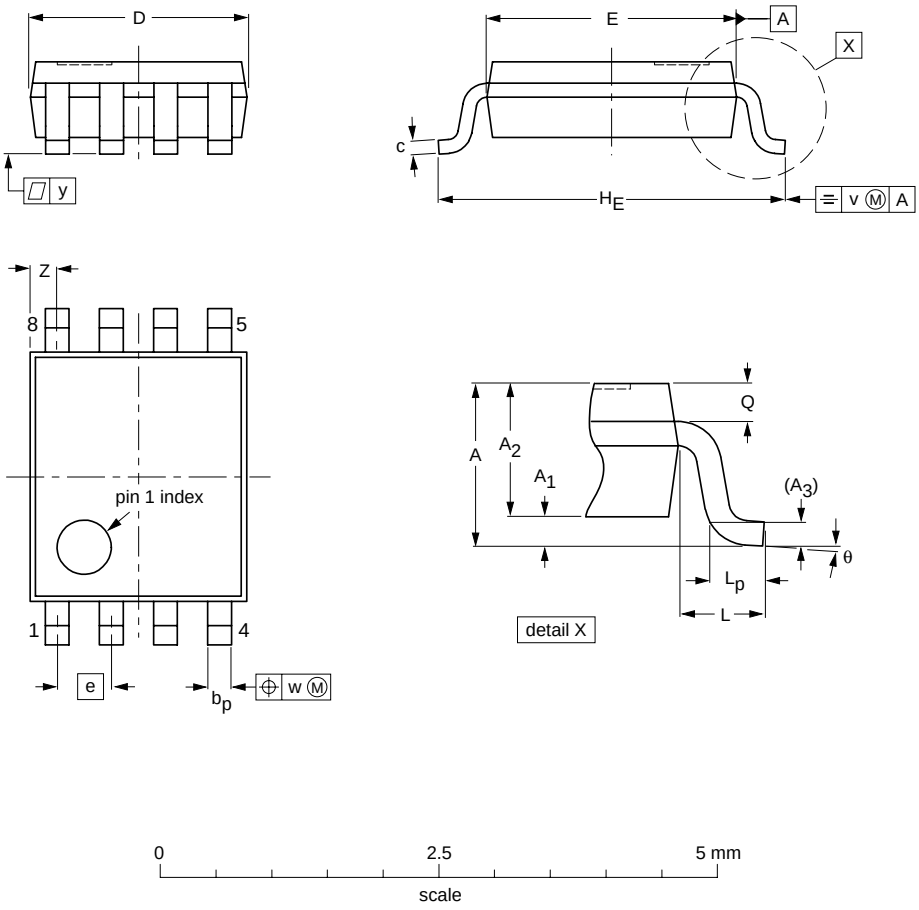
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Fig 10. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

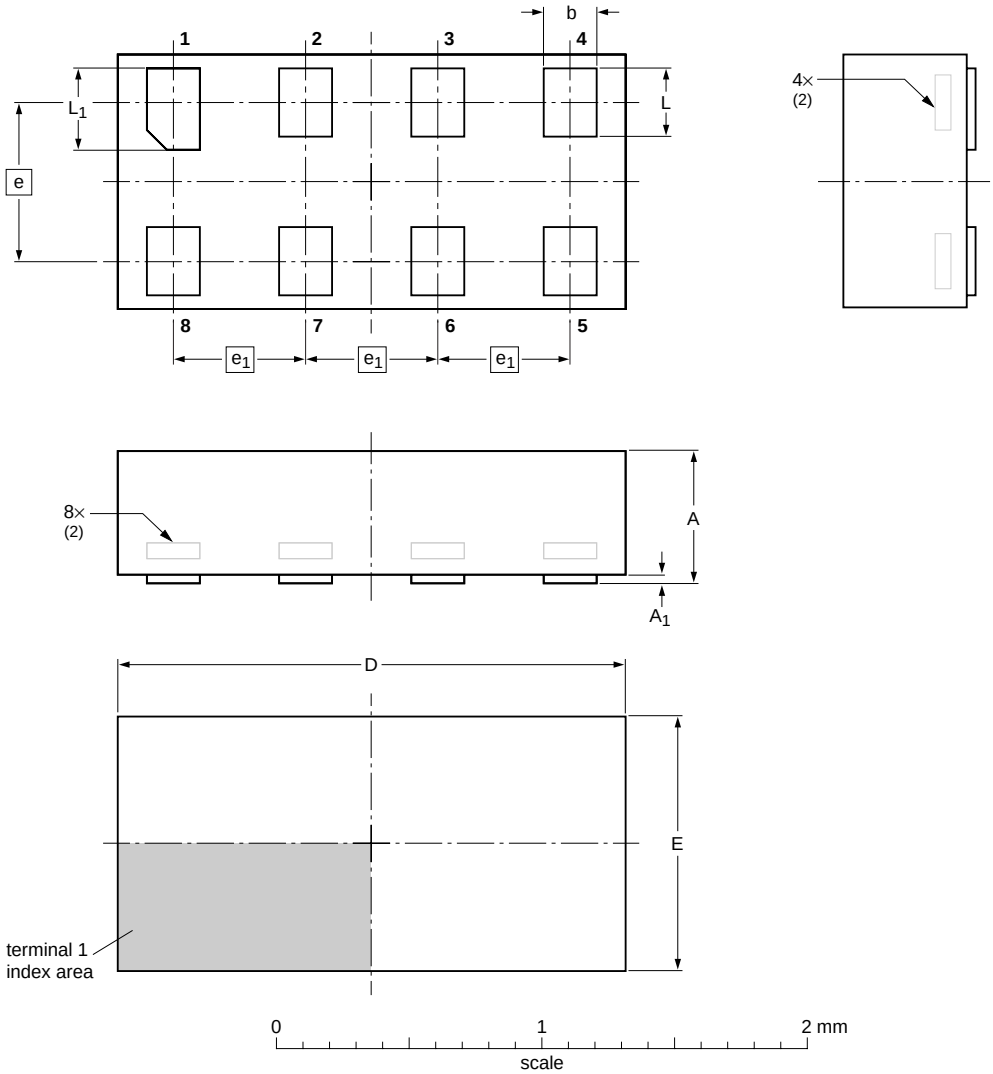
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

Fig 11. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm **SOT833-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A1 max	b	D	E	e	e1	L	L1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

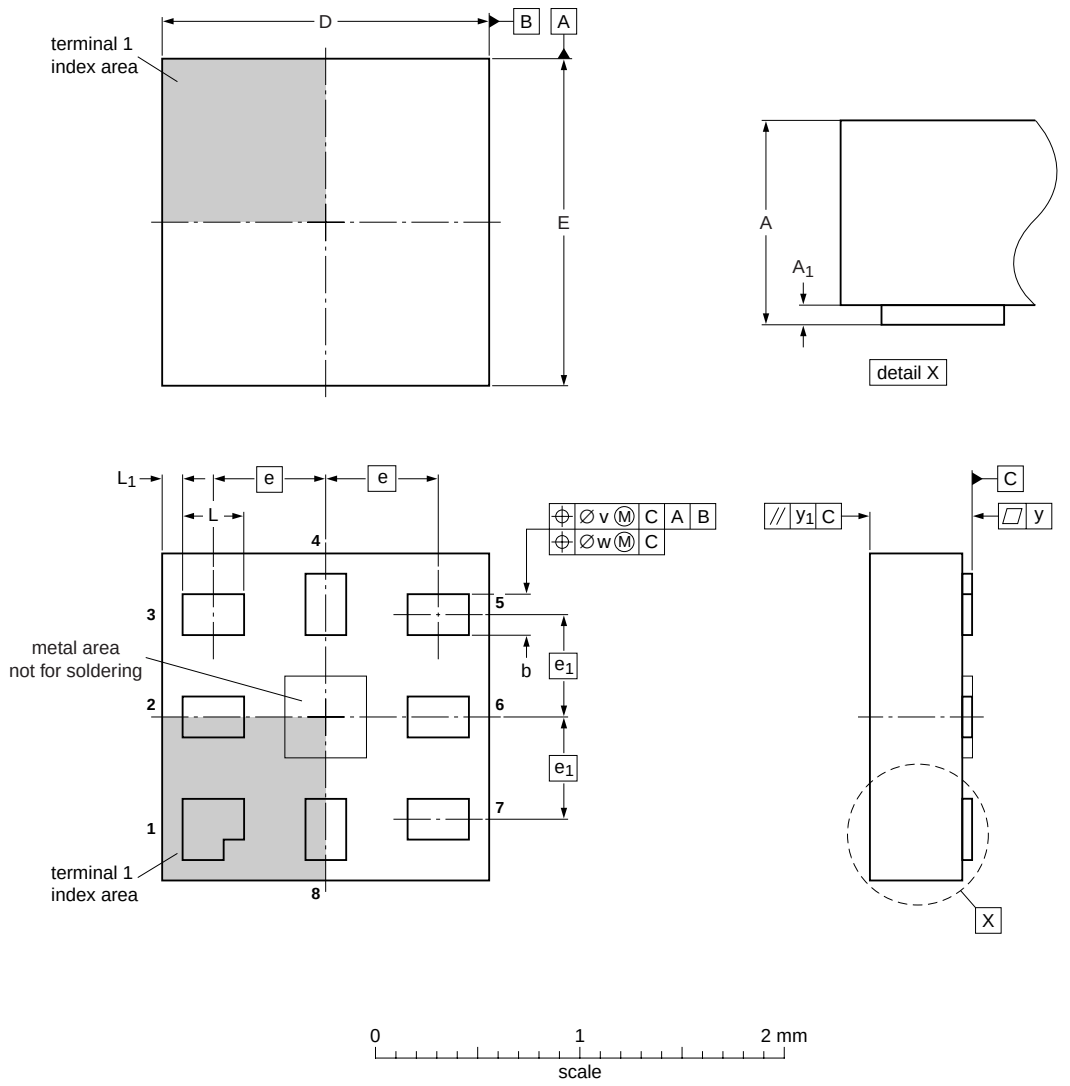
Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~07-11-14~~ 07-12-07

Fig 12. Package outline SOT833-1 (XSON8)

XQFN8U: plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 x 1.6 x 0.5 mm **SOT902-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	b	D	E	e	e_1	L	L_1	v	w	y	y_1
mm	0.5	0.05 0.00	0.25 0.15	1.65 1.55	1.65 1.55	0.55	0.5	0.35 0.25	0.15 0.05	0.1	0.05	0.05	0.05

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT902-1	- - -	MO-255	- - -			~~05-11-25~~ 07-11-14

Fig 13. Package outline SOT902-1 (XQFN8U)

14. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
TTL	Transistor-Transistor Logic
HBM	Human Body Model
ESD	ElectroStatic Discharge
MM	Machine Model
DUT	Device Under Test

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G74_6	20080219	Product data sheet	-	74LVC1G74_5
Modifications:	• Figure 13: package outline drawing updated to latest version • Figure 1 and Figure 2: pin numbers removed from logic symbols			
74LVC1G74_5	20070809	Product data sheet	-	74LVC1G74_4
74LVC1G74_4	20061207	Product data sheet	-	74LVC1G74_3
74LVC1G74_3	20050201	Product specification	-	74LVC1G74_2
74LVC1G74_2	20040909	Product specification	-	74LVC1G74_1
74LVC1G74_1	20040202	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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